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FORMATION
ALLEGRO FPGA SYSTEM PLANNER

Filière Placement & Routage Cadence (PCB Design Environnent)

Ref : ALL-FPGA

Training Category
Front End

Duration
2 days

Prerequisites
You need to have experience with or already have knowledge of Logic Design.

Learning Objectives
After completing this course, you will be able to:
- Identify how data flows from the FPGA System Planner (FSP) to the schematic and PCB
- Create a design in FSP
- Define the protocols and interfaces in an FSP design
- Synthesize the connections in FSP protocols and interfaces
- Add terminations and external ports in an FSP design
- Generate an Allegro Design Entry HDL schematic from your FSP design
- Export your FSP placement to the PCB Editor
- Back annotate pin swaps and design changes from the schematic and PCB Editor to FSP

Course Agenda

Day 1
- FPGA System Creation
- FPGA System Synthesis
- FPGA System Completion

Day 2
- Integration with Allegro Design Authoring and PCB Editor
- Postlayout Optimization
- Importing FPGA Constraint Files and Virtual Interfaces
- FSP Models

Audience
Design Engineers - FPGA Designers - PCB Designers

Le formateur dispense cette formation en français et éventuellement en anglais sur un des sites Européen de Cadence Design Systems Inc