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FORMATION ALLEGRO HIGH-SPEED CONSTRAINT MANAGEMENT V16.6-2015

Filière Placement & Routage Cadence (PCB Design Environment)

Ref : ALL-HSC

Course Description

SThis Engineer Explorer course is designed around advanced topics and exploration of the software. This course does not cover basic operations. If you are not actively using the software, then you need to complete the Allegro PCB Editor, the Allegro® Package Designer, or the Allegro Design Entry HDL Front-to-Back Flow course.
In this course, you apply and verify high-speed constraints across a design process. You learn to schedule nets, control impedance on nets, control the propagation delay from your drivers to receivers, and match the propagation delay of driver and receiver pairs.

Duration

2 days

Prerequisites

You must have experience with or knowledge of Allegro PCB Editor, Allegro Package Designer, or Allegro Design Entry software.

Learning Objectives

- Define specific net scheduling of high-speed nets
- Match the propagation delay of nets and connections
- Define minimum and maximum propagation delays for nets and connections
- Identify high-speed constraint violations
- Identify all the high-speed constraints that you can apply to the nets in your designs
- Create spacing and physical constraints as well as area constraints and class-to-class rules
- Customize worksheets
- Create formula-based constraints
- Create customized constraints using the SKILL® programming language

Course Agenda

Day 1

- Database setup
- User-defined net scheduling
- Propagation delay
- Relative propagation delay
- Impedance constraints

Day 2

- Total etch-length constraints
- System constraints
- Physical and spacing constraints
- Formula-based constraints
- Custom constraints

Le formateur dispense cette formation en français et éventuellement en anglais sur un des sites Européen de Cadence Design Systems Inc