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# FORMATION
# ALLEGRO PCB SI FOUNDATIONS
## Filière Placement & Routage Cadence
## (PCB Design Environment)
## Ref : ALL-SI

### Training Category
System Interconnect Design – Allegro & OrCAD

### Duration
3 days

### Prerequisites
Familiar with digital and analog circuit design methodology
A working knowledge of PCB signal analysis and transmission line theory

### Learning Objectives
- After completing this course, you will be able to:
- Create, extract, and explore topologies
- Run solution space analysis
- Create an electrical constraint set
- Apply constraints to drive placement and routing
- Run postroute DRC check
- Use template revision to update the ECSet applied to the nets
- Analyze the routed board design for signal integrity
- Create a DesignLink between boards and use it to run multiboard
- simulation Course Agenda

### Course agenda
Day 1
- Allegro PCB SI design flow Board setup requirements DC net connections
- Model assignment Default and discrete models Model integrity IBIS to DML translation

Day 2
- Net extraction SigXplorer basics
- Simulation with SigXplorer Sweep simulations Trace models Constraint floorplanning Constraint DRCs

Day 3
- DRC routing Creating a DesignLink System analysis Postroute analysis
- Reflection and crosstalk simulation Postroute bus analysis Differential pairs

### Audience
Electrical Engineers PCB Designers

*Le formateur dispense cette formation en français et éventuellement en anglais sur un des sites Européen de Cadence Design Systems Inc*