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FORMATION ALLEGRO PCB SIGRITY SI FOUNDATIONS V16.6

Filière Placement & Routage Cadence (PCB Design Environment)

Ref: ALL-SIG

Training Category
System Interconnect Design – Allegro & OrCAD

Duration
2 days

Prerequisites
Familiar with digital and analog circuit design methodology
A working knowledge of PCB signal analysis and transmission line theory

Learning Objectives
After completing this course, you will be able to:
- Create, extract, and explore topologies
- Run solution space analysis
- Create an electrical constraint set
- Apply constraints to drive placement and routing
- Run postroute DRC check
- Use template revision to update the ECSet applied to the nets
- Analyze the routed board design for signal integrity
- Create a DesignLink between boards and use it to run multiboard
- simulation

Course Agenda
Day 1
- Allegro PCB SI design flow
- Board setup requirements
- Model assignment
- Default and discrete models
- IBIS to DML translation
- Net extraction
- Simulation with SigXplorer

Day 2
- Sweep simulations
- Trace models
- DRC routing
- Creating a DesignLink
- Postroute analysis
- Reflection simulation
- Differential pairs

Audience
Electrical Engineers
PCB Designers