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FORMATION
SIGRITY SYSTEMSI FOR PARALLEL BUS AND SERIAL LINK ANALYSIS

Filière Placement & Routage Cadence (PCB Design Environment)

Ref: ALL-SIGPBSLA

Training Category
Front End

Duration
3 days

Course Description
This course covers modeling, simulation and analysis of parallel bus systems, and serial link systems using Sigrity™ SystemSI™.
On first day, the course covers modeling, simulation and analysis of simple DDR3 and DDR4 parallel bus systems (DDR3-SPBS and DDR4-SPBS) without a power distribution network. You will build block-level models of DDR3-SPBS and DDR4-SPBS, set up timing budget and analysis options for the DDR3-SPBS, including channel simulation options for the DDR4-SPBS. Next, simulate DDR4-SPBS and then DDR3-SPBS, with/without on-die parasitics, package parasitics and sweeping several circuit parameters. You will generate reports with tables and analyze waveforms to evaluate the signal integrity performance of these systems.
On the second day, this course covers modeling, simulation and analysis of power-aware DDR3 and DDR4 parallel bus systems (DDR3-PAPBS and DDR4-PAPBS). You will build DDR3-PAPBS and DDR4-PAPBS with S-parameters model of the power-aware parallel bus interface, assigned to the PCB block of these systems. You will first simulate DDR3-PAPBS with non-ideal power, with/without on-die parasitics, package parasitics and sweeping several parameters. You will analyze simulation based reports and waveforms to evaluate the power and signal integrity performance of the DDR3-PAPBS. Next, you will simulate the DDR3-PAPBS with broadband circuit model of the DDR3 interface assigned to the PCB block, generate reports and evaluate its power and signal integrity performance. You will also model, simulate and analyze the performance of the DDR3-PAPBS with two memory blocks. Finally, you will build a DDR4-PAPBS included with the package models for controller and memory. You will simulate the DDR4-PAPBS with non-ideal power, with/without on-die parasitics, package models, etc., generate simulations results and perform comparative evaluation of power integrity and signal integrity performance of the DDR4-PAPBS.
On day three, this course covers modeling, simulation and analysis of pre-layout and post-layout serial link systems (SSLS). You will build an SSLS, set up channel analysis options, run several simulations, generate reports and perform comparative signal integrity performance evaluations of the SSLS. Next, you model and run several simulations of the SSLS included with AMI models of the transmitter and receiver and analyze simulation results for comparative signal integrity performance evaluations of the SSLS.

You will modify the SSLS, using IBIS-Transmitter and IBIS-Receiver models, run several sweep mode simulations and explore effects of different types of IBIS-AMI transmitter on the signal integrity performance of the modified SSLS. Next, you modify the SSLS to create a pre-layout serial link system (PL-SLS), with a W-element model of the channel and the S-parameters model of vias, generated using the Via Wizard tool. You will perform several simulations to explore effects of vias and W-Element parameters on the signal integrity performance of the PL-SLS. Finally, you will perform simulation and analysis of a serial link system to explore crosstalk effects, in terms of the signal degradation of the primary serial link, due to coupled serial links.
On day three this course also covers debugging problems in SystemSI, using several examples.

Prerequisites

A practical understanding of power and signal integrity issues of high-speed parallel bus systems
Basic understanding of transmission lines and S-parameters

Learning Objectives

After completing this course, you will be able to:

- Build a block-level topologies of parallel bus systems (PBSs) in the System SI-PBA II tool and serial link systems (SLSs) in the SystemSI-SLA II tool.
- Assign IBIS models to the functional blocks of the PBSs and SLS.
- Generate W-Element transmission line model to represent pre-routed parallel bus or serial link interfaces.
- Connect blocks of PBSs and SLSs, using the model connection protocol (MCP).
- Set analysis options, including channel simulation options before simulating these PBSs and SLSs.
- Set voltage and current probe points in PBSs and SLSs.
- Set various types of sweeping parameters.
- Run simulations and sweep simulations.
- Generate simulation based reports with tables and waveforms.
- View tables, 2D plots, Eye Diagrams, BER Eye plots, Bathtub plot, impulse and ramp responses of channel, etc.
- Analyze simulation-based results, waveforms and tables to evaluate the power and signal integrity performance of the PBSs and SLSs.
- Modify the PBSs by replacing the S-parameters model of the parallel bus interface by its broadband circuit model, by adding another memory block(s), by replacing IBIS models of the controller and memory blocks, etc.
- Modify SLSs by adding AMI models or by adding IBIS-AMI models to transmitter and receiver blocks, adding Via models, generated by the built-in Via Wizard etc.
- Use the built-in serial link system template for crosstalk analysis for exploring signal degradation of the primary serial link channel due to other coupled serial links.
- Run simulation of the modified PBSs and SLSs and generate simulation based results.
- Compare power and signal integrity performance of the modified PBSs and SLSs, based on the waveforms, timing parameters in the tables of the generated reports.

Audience

Electrical engineers and PCBdesigners involved with design-oriented modeling, simulation andanalysis of pre-routed and post-routed high-speed parallel bussystems (DDR3/DDR4), and serial link systems (SerDes).

Le formateur dispense cette formation en anglais sur un des sites Européen de Cadence Design Systems Inc