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FORMATION ALLEGRO SIGRITY PI

Filière Placement & Routage Cadence (PCB Design Environment)

Ref: ALL-SIGPI

Training Category
System Interconnect Design – Allegro & OrCAD

Duration
1 day

Prerequisites
You must have experience with or knowledge of the following:
Printed Circuit Board Design

Learning Objectives
- After completing this course, you will be able to:
- Set up a board database for analysis
- Perform static IR-drop analysis
- Create and verify place current density constraints
- Create and verify sink voltage constraints Create and verify via current constraints
- Create voltage and current probes to measure DC voltage and current
- Create decoupling configurations in the Power Feasibility Editor
- Define Power Integrity Constraint Sets that are stored and maintained in the Constraint Manager
- Place decoupling capacitors based on the templates from the Power Integrity Constraint Sets

Course Agenda
- Introduction to DC Analysis
- Static IR Drop Analysis
- PowerDC Constraints
- The Power Feasibility Editor Power Integrity
- Constraint Sets Power Integrity
- Constraint driven placement

Audience
Analog Designers - Design Engineers - Electrical Engineers

Le formateur dispense cette formation en français et éventuellement en anglais sur un des sites Européen de Cadence Design Systems Inc