CENTRE DE FORMATION AGRÉÉ
1 bis, avenue Foch – 94100 Saint-Maur – France
Tél.: +33 (0)1 70 91 67 20
Fax: +33 (0)1 70 91 67 29
info@artedas.fr
www.artedas.fr

FORMATION ALLEGRO SIGRITY POWER INTEGRITY SUITE

Filière Placement & Routage Cadence (PCB Design Environment)

Ref: ALL-SIGPIS

Training Category Duration Prerequisites Learning Objectives
Front End

Duration
1 day

Prerequisites
You must have experience with or knowledge of the following:
Printed Circuit Board Design.

Learning Objectives
After completing this course, you will be able to:
- Set up a board database for analysis
- Perform static IR-drop analysis
- Graph the impedance of the power distribution network across a complete frequency bandwidth
- Assign capacitor models to an existing printed circuit board
- Create and edit capacitor models
- Optimize capacitor selection for performance and cost

Course Agenda
- Introduction to Sigrity Power Integrity Suite
- Database Translation
- Static IR-drop Analysis
- Power Plane Impedance Analysis
- Capacitors and Plane Analysis Simulation
- Capacitor Optimization

Audience
Analog Designers - Design Engineers - Electrical Engineers