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FORMATION ALLEGRO SIGRITY POWER DC AND OPTIMIZE PI

Filière Placement & Routage Cadence (PCB Design Environment)

Ref: ALL-SIMGAP

Course Description

This course first discusses building a simple pre-layout PCB in PowerSI® followed by studying electrical parameters of signal traces reported in the Trace Properties window. Next, electrical parameters of microstrip and stripline traces reported in the Trace Properties window and computed using the closed form expressions are compared. Next, the process of generating S-parameters model for power and signal nets of the simple pre-layout PCB, computing impedance parameters and loop inductances of power and signal nets are discussed in this course. Next, the methodology of generating electrical models of power-aware parallel bus, with and without DECAPS on a real-world PCB, is discussed, using PowerSI and Broadband SPICE tools. Process of analyzing PowerSI generated S-parameters data of the power-aware parallel bus interface, in terms of return loss and insertion loss, computing open-circuit and short-circuit impedance parameters and evaluating power and signal integrity performance of the post-routed parallel bu interface is discussed in this course. Computation of short-circuit impedances of power nets by shorting the VRM port or by terminating the VRM port using series/parallel R-L-C circuit and also by using the VRM impedance is discussed in this course.

Next, the methodology of generating electrical models of a serial link interface, using PowerSI and the 3D-EM tools is discussed. You will analyze PowerSI, as well as, 3D-EM generated S-parameters data of the serial link interface with or without signal and ground via stubs, in terms of return loss and insertion loss parameters. Also, the methodology of generating electrical models of a serial link interface, using the built-in cut-and-stitch (CAS) process in the 3D-EM tool is discussed in this course. Finally, S-parameter model generation of a differential pair of vias using the 3D-EM tool, followed by analyzing signal integrity performance of differential vias with or without via stubs, in terms of insertion loss parameters, is discussed in this course.

Duration

2 days

Prerequisites

You must have experience with or knowledge of the following:

- PCBs, transmission lines, S-parameters, and
- Practical understanding of power and signal integrity issues in high-speed digital systems

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Learning Objectives

After completing this course, you will be able to:
Use PowerSI, Broadband SPICE and 3D-EM tools to generate electrical models (S-parameters and broadband SPICE circuit) of pre/post routed high-speed interfaces on PCBs and perform detailed frequency domain analysis for evaluating power and signal integrity performance of these interfaces.

Audience

Engineers involved in PCB and IC-package development based on electrical model generation and frequency-domain analysis for power and signal integrity performance evaluations of high-speed interfaces and digital systems.

Le formateur dispense cette formation en anglais sur un des sites Européen de Cadence Design Systems Inc