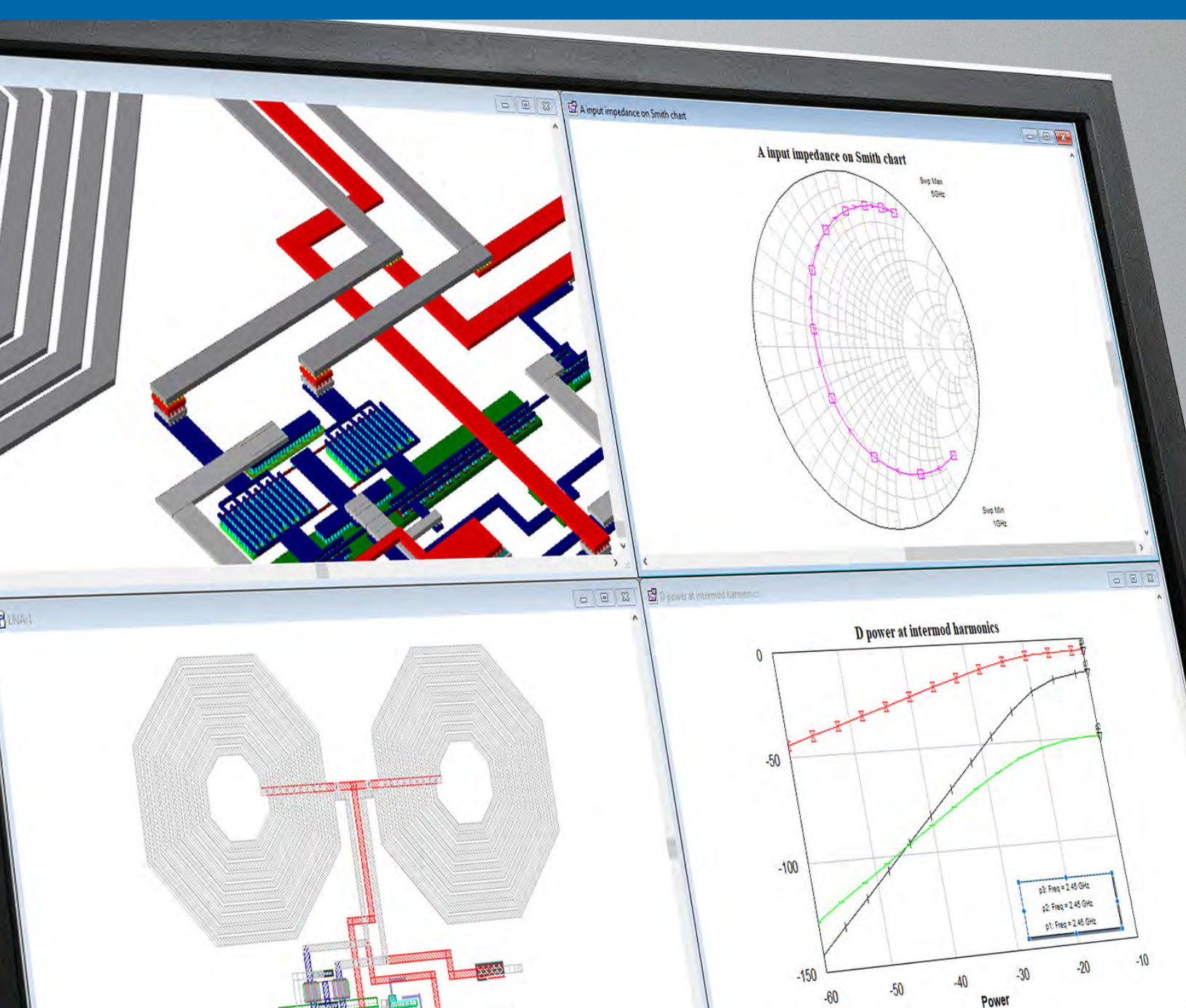# Analog Office

Analog/RFIC Circuit Design Software

cādence®

Analog Office

RFIC/Analog IC Design Software

Analog Office offers designers of small-scale and RF front-end functional blocks within large-scale silicon RFICs and analog ICs an intuitive, flexible, and accurate design solution. Analog Office, along with Microwave Office, Visual System Simulator™ (VSS), AXIEM, and Analyst™ software tools operate within the AWR Design Environment platform. The unique software architecture streamlines designs and increases user productivity as it lets designers control and integrate best-in-class tools to capture, synthesize, simulate, optimize, lay out, extract, and verify RFIC and analog designs from the system level through to final tape-out. Analog Office is the ideal design tool for PC-based organizations designing RF/analog electronics using mature silicon processes.

AWR Design Environment
Microwave Office
Visual System Simulator
Analog Office
AXIEM
Analyst

Advantages

RF Focused

A powerful RFIC design platform that enables fast and accurate entry of design concepts, supporting design management with parasitic-aware component models, analyses, and design assistance that helps engineers study and understand the interdependencies of analog, RF, and mixed-signal design.
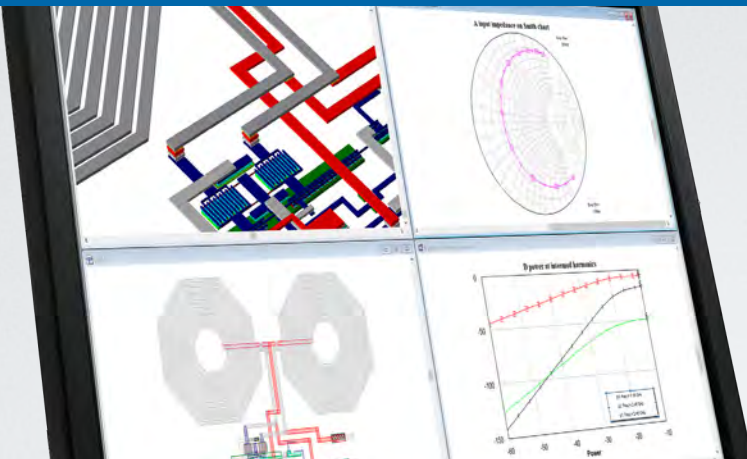
Parasitic Extraction

Analog Office works with iNet and ACE technologies to perform interconnect modeling and parasitic extraction of IC structures created with the integrated layout editor.

Interoperability

Analog Office is fully integrated within the AWR Design Environment open platform, allowing designers to exchange design data between third-party IC layout and EM simulation tools. The Open Access import/export wizard transfers design schematic data between Analog Office and Cadence Virtuoso, streamlining the transfer of IP between tools.

"Analog Office provided the design team with a significant advantage by supporting our own custom PCells to work in tandem with the authorized foundry kit, improving the accuracy of the layouts and enabling complex structures to be drawn efficiently."

— Leigh Milner, Microelectronics Research Defence Science and Technology Group

Features at a Glance

- Schematic/Layout – Design entry with industry-leading tuning
- APLAC – Linear and nonlinear circuit simulation
- Parasitic Extraction – Fully integrated EM analysis
- DRC/LVS – Design rule checking/layout vs. schematic
- PDKs – Process design kits (PDKs) from leading silicon foundries

Capabilities

Design Entry – The intuitive user interface is tailored to project management and design entry for high-frequency circuits, allowing engineers to quickly build networks from a comprehensive library of RF-aware components and transmission lines supporting parameterization for tuning/optimization, and hierarchical design supporting circuit, system and EM co-simulation with simulation controls and result graphs for standard and user-customized RF/microwave measurements.

RFIC Design Flow – Provides comprehensive simulation of RFIC technologies from initial concept to final tapeout. The RF/microwave-aware active and passive device models, silicon foundry PDKs, and support for Spectre netlist simulation accurately capture the behavior of RF front-end blocks to an RFIC design. Analog Office works either as a stand-alone tool or as supplemental simulation software within a Cadence Virtuoso design flow.

Silicon PDKs – PDKs for leading silicon foundries are developed for the open AWR Design Environment platform from foundry-supplied technology files, device models, and design rules. These PDKs are subjected to extensive validation at both cell and circuit level to ensure quality and conformance to best-in-class design methodologies for high-frequency RFIC designs, accelerating silicon tapeouts and enabling first-pass success.
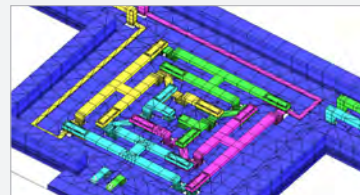
Simulation

APLAC – Provides frequency-domain, harmonic balance, and transient simulations for small-scale RFICs and RF front-end blocks within large-scale RFICs to efficiently predict the performance of high dynamic range RF circuits operating at RF, microwave, and millimeter-wave frequencies for wireless communication and radar applications.

Planar EM – AXIEM and/or OEA International's Net-AN provides the speed and accuracy to characterize and optimize passive structures, transmission lines, and spirals as well as RFIC packaging.

Verification

Wireless Conformance Tests – Simulate the performance and functionality of any wireless RFIC device in accordance with all main cellular communications (5G, LTE, and more), wireless connectivity, and broadband standards through circuit/system co-simulation with VSS pre-configured communication test benches for transmitter conformance testing and receiver sensitivity analysis.


Small-Scale RFICs
An ideal platform for small-scale (low-to-moderate number of active/passive on-chip devices) RFIC design entry, project management, simulation and post-processing of results for silicon-based devices.
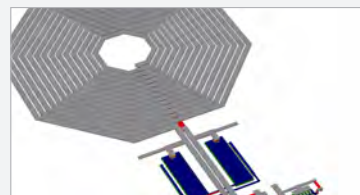
RF Blocks Within Large-Scale RFICs
Co-simulation of Spectre and HSPICE generated netlists along with imported OpenAccess schematics from Cadence and Synopsys supports detailed analysis of radio blocks from large-scale RF/mixed-signal RFICs.
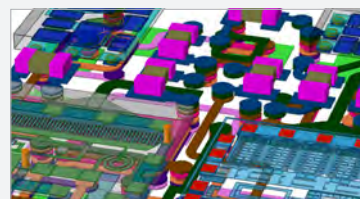
Multi-Chip Modules
The software's hierarchical framework supports simulation of diverse MMIC, RFIC and PCB processes, multi-layer interconnects, embedded passives, and surface-mounted mini-devices found within multi-chip RF modules.

Services and Support

Technical Support
Get started faster or work through tough issues by contacting AWR software support engineers who are ready to help via phone and email during normal business hours.

Technical Resources
Access volumes of self-help information at awr.com/support, including application tips, example projects, user forum, and more.

Online Training
Get a jump start with self-paced modular training videos on awr.com/elearning that aim to educate new users on AWR software.

Academic Resources
AWR software donations are available to support academic institutions with an emphasis on teaching and/or non-proprietary research.

AWR Learn more at awr.com

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