Allegro Sigrity SI

Streamlining the creation of high-speed interconnect on digital PCBs and IC packages

The Cadence® Allegro® Sigrity™ signal integrity (SI) integrated high-speed design and analysis environment streamlines creation of high-speed interconnect on digital printed circuit board (PCB) systems and IC packages. A range of capabilities—from basic to advanced—enable designers and electrical engineers to explore, optimize, and resolve issues related to electrical performance at all stages of the design cycle. By enabling an electrical constraint-driven design flow, this unique environment accelerates the time to design success while reducing the overall cost of end products.

Allegro Sigrity SI Solution

Cadence Allegro Sigrity SI provides a scalable, cost-effective pre- and post-layout system interconnect design and analysis environment. Included are both first-order and advanced analysis for the board, package, and system levels. The Allegro Sigrity SI base integrates tightly with Cadence PCB and IC package layout editors, and Cadence Allegro Design Authoring—enabling front-to-back, constraint-driven, high-speed PCB and IC package design.

Allegro Sigrity SI addresses the design challenges presented by increasing design density, faster data throughput, and shrinking product design schedules by enabling designers to address high-speed issues throughout the design process. This approach allows design teams to eliminate time-consuming iterations at the back-end of a design process.

Modeling of the I/O buffer is accomplished by using the IBIS modeling standard. Transistor-level models can be converted to power-aware IBIS models, enabling transistor-level accuracy in a fraction of the simulation time.

Modeling interconnect is accomplished through multiple methods. Depending on the detail available and the expertise of the user, signals can be modeled with ideal transmission line parameters defined by the user or with extracted S-parameters using 3D-full-wave field solvers and a number of methods in between. Utilizing both buffer models and interconnect models, analysis can be performed early to refine design intent, during the design process to validate progress, and as the design is finalized to ensure electrical specifications are met.

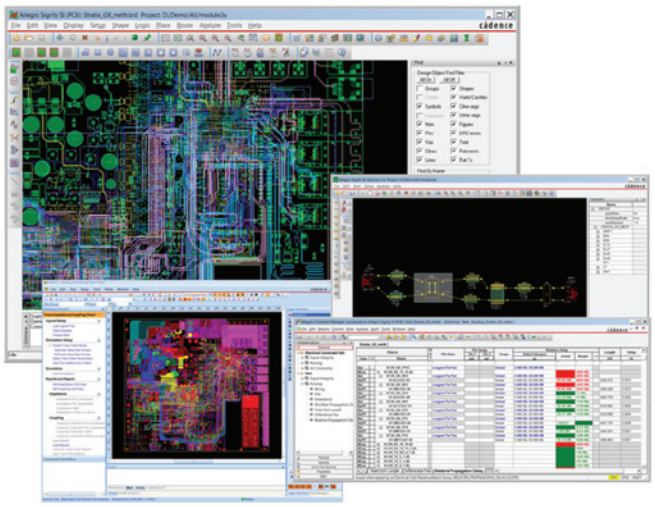

Figure 1: Electrical constraints guide the design process and reduce design iterations. SI analysis can be performed throughout the design process with signal, power, and ground coupled together for final signoff.

Key Capabilities

- Highly integrated design and analysis environment removes the need for error-prone and time-consuming manual design translation
- Intuitive pre-route analysis tools enable a design methodology that streamlines post-route design verification through a consistent front-to-back electrical constraint management environment
- Timing budgets of complex source-synchronous parallel interfaces can be efficiently and accurately validated with power-aware analysis that considers simultaneous switching noise (SSN)
- Serial-link design methodology support pre- and post-route techniques that guide physical implementation, screen routed designs, and guide the designer to the appropriate signals to perform fast, accurate, and detailed million-bit simulations using the latest industry-standard IBIS-AMI SerDes models
- IC package designs are easily assessed for design quality and characterized for use in die-to-die system analysis

Features

The Allegro design canvas features included with Allegro Sigrity SI can be used to both view and modify a design as analysis is performed on an Allegro PCB or IC package design. In addition, users can start with a blank canvas, mock up a design, and perform what-if power-aware analysis to learn early how signal, power, and ground
will interact with different stackup configurations.

Integrated high-speed design and analysis

To eliminate the risk of design translation issues, Allegro Sigrity SI is seamlessly integrated with the Allegro PCB and IC package layout editors and allows for constraints and models to be tightly integrated with the design file. The integrated design and analysis system is aware of multi-net electrical constructs from logical design authoring to physical implementation. For example, differential pairs and extended nets (nets with a series termination) are recognized,

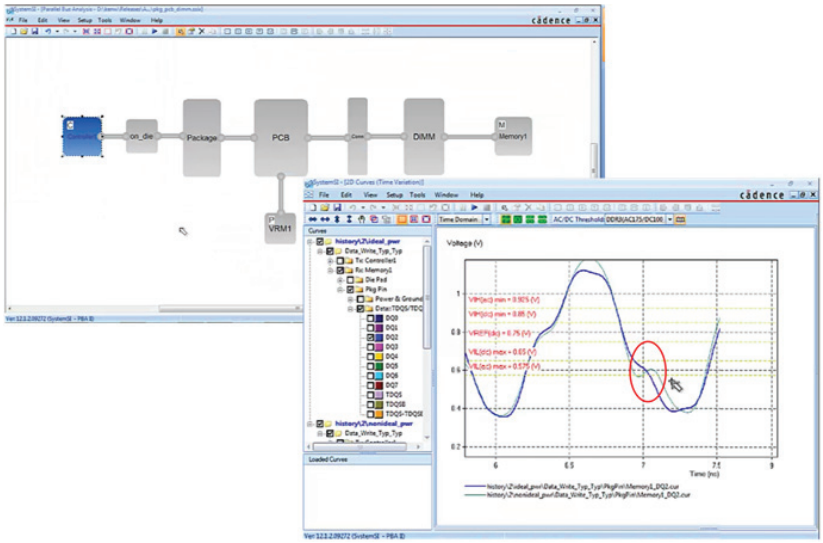

Figure 2: SI analysis with ideal power and ground (blue) compared to SI analysis with non-ideal power and ground (green). Analysis with ideal power and ground may create a false sense of security. Analysis with non-ideal power and ground catches ringback and timing push-out issues.

extracted, and simulated as one electrical net from either schematic or layout. The SigXplorer module integrates with logical or physical design tools and provides a graphical view of I/O buffers, transmission lines, and vias such that complex topologies can be modified in a what-if fashion without having to change the actual design. SigXplorer also allows engineers to sweep various parameters within the topology to identify a topology solution space, which can then be captured in the constraint management system and guide PCB designers to first-pass electrical compliance. I/O buffers can be modeled using industry-standard IBIS and SPICE models (encrypted or unencrypted).

Parallel bus design and power-aware SI analysis methodology

Allegro Sigrity SI provides a detailed and thorough methodology to perform analysis of all the signals associated with a source-synchronous bus such as DDR3. Utilizing a four-step process, the time to accurately simulate various configurations (read/write, active, idle) associated with the functioning of source synchronous buses with or without on-die termination (ODT) is shortened. These steps are as follows:

1. Power-aware IBIS models are converted from transistor-level models. These IBIS 5.1-compliant models provide the same level of accuracy as transistor-level models, but simulate 50 to 100 times faster than the transistor-level version.
2. Interconnect modeling is performed using fast and accurate hybrid solver technology or with detailed 3D full-wave solving technology. All extractions include signal, power, and ground coupled together.
3. Interconnect and I/O models are connected together in a topology canvas. Interconnect models may consist of chip, package, board, connector, or cable models. These interconnect models may be either simple pre-route transmission lines or the detailed extractions discussed in Step 2. Using Model Connection Protocol (MCP) headers in the interconnect models, each fabric can be intuitively connected to the proper signals in the connecting fabric. The graphical user interface (GUI) allows for a simplified way of cascading S-parameter interconnect models of each part of the system (e.g., package, PCB, DIMM) and connecting signal, power, and ground from each model together using a spreadsheet-type interface enabled through MCP.
4. Parallel bus analysis is performed using the power-aware connected models discussed in Step 3. The simulation

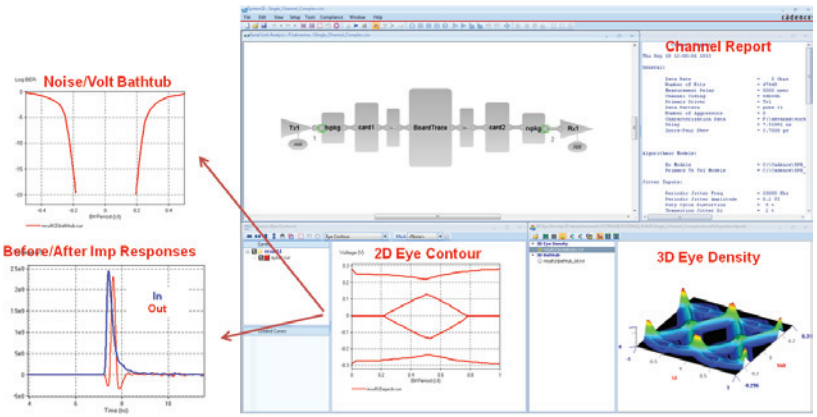

Figure 3: SI for serial data channels includes IBIS-AMI models to represent the transceivers, as well as sophisticated modeling techniques for all fabrics (chip-package-board) of the topology. Results are reported in 2D, 3D, and in HTML report formats.

fully considers SSN. The simulation is aware of DDR3 test and measurement criteria and (based on slew rate) properly derates setup and hold margins through user-defined derating tables for different signals in the source synchronous bus.

The simulation results are captured and post processed according to the parallel bus standard (e.g., DDR3). Timing checks are made between signals such as data and strobe and anything out of spec is highlighted in the waveform display.

Serial link design and analysis methodology

When engineers face today's demands for faster data throughput, each section of the interface takes on greater complexity. Transceivers feature dynamic equalization and clock and data recovery algorithms that require advanced modeling techniques. IC package and PCB interconnect models must be extracted with more accuracy than ever before in order to accurately characterize interconnect from die to die. Interconnect structures must be carefully characterized so signal loss, frequency-dependent materials, and impedance discontinuities are all accurately represented through broadband S-parameter interconnect models. The Allegro Sigrity SI solution provides a detailed and thorough methodology (similar to the parallel bus methodology described in the previous section) to perform analysis of all the signals associated with a high-speed serial data channel. The time to accurately simulate and establish compliance is accelerated with the following four steps:

1. IBIS-AMI models are connected to the transceivers. These IBIS 5.1-compliant models provide the ability to optimize parameters based on the channel that will be simulated.
2. Interconnect modeling is performed using fast and accurate hybrid solver technology or with detailed 3D full-wave solving technology. All extractions include signal, power, and ground coupled together.
3. Interconnect and I/O models are connected together in a topology canvas. Interconnect models may consist of chip, package, board, connector, or cable models. These interconnect models may be either simple pre-route transmission lines or the detailed extractions discussed in Step 2. Using MCP headers in the interconnect models, each fabric can be intuitively connected to the proper signals in the connecting fabric. The GUI allows for a simplified way of cascading S-parameter interconnect models of each part of the system (e.g., package, PCB) and connecting signal, power, and ground from each model together using a spreadsheet-type interface enabled through MCP.
4. Channel analysis is performed using the IBIS-AMI buffer models and coupled signal, power, the interconnect models discussed in Step 3. Noise can be injected into the VRM to allow the simulation to consider less than ideal power and ground.

The simulation results are captured and post processed according to the selected serial link standard (e.g., PCI Express® 3.0). Compliance checks are made and collected into an easy-to-read HTML report file.

IC packaging assessment and model extraction methodology

Allegro Sigrity SI provides an environment for the assessment, characterization, and simulations of IC package (.mcm or .sip) interconnect. Engineers can make tradeoffs to minimize cost while maximizing performance of the package module interconnect.

The electrical-assessment features are most commonly used by the package designer to gain a quick first-order evaluation of the electrical quality of the package design. Available as part of the assessment capability is signal analysis (trace impedance and coupling checks), power/ground analysis (net-pair and per-pin properties), and DC current analysis (DC current and IR drop analysis). The assessment capability is accomplished with minimal electromagnetic expertise. HTML-based reports can be created showing the level of analysis that has been performed along with the results.

The IC package assessment and model extraction methodology can prove particularly valuable when package design is outsourced. The electrical performance assessment features provide a quick and thorough means to assess the package design, which reduces the time before providing feedback to the package designers. When the assessment provides good results, the extraction technology provides an efficient means for developing either full-package models or highly accurate package-section models for use in high-frequency system-level time-domain simulation.

For more advanced analysis, package characterization engineers have access to integrated hybrid (2D/3D) and full-wave 3D field solver engines. These solvers can be used to create full-package models

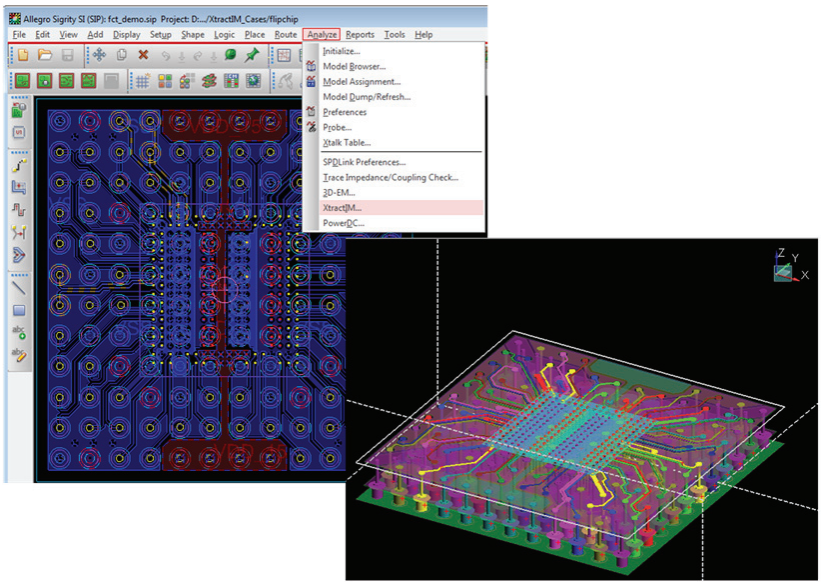

Figure 4: Package assessment and extraction is tightly integrated with the package design environment. A first-order assessment can be accomplished to provide quick feedback of the overall package performance. Detailed full-package models or 3D package sections can be extracted. The solution is rounded out with IR drop and thermal analysis capability.

or a smaller section of the package can be extracted to create high-fidelity S-parameter models. These models can be analyzed independently or passed off to system analysts to include the package model in their system topologies.

In addition, thermal and thermally aware IR drop analysis is available as part of the solution.

Virtual prototyping environment

Engineers can evaluate placement strategies when used in conjunction with Allegro design authoring tools, and assign design intent by embedding constraints in the front-end design database. In addition, physical layouts can be quickly mocked up and advanced analysis can be performed to enable optimization. These physical structures can be shared with PCB and IC- package designers to communicate physical design intent.

The value of the virtual prototyping environment can be seen in memory interface analysis. To understand the effects of SSN, structures that include power, ground, and a memory bus must be constructed. With these structures, which can be constructed in the Allegro Sigrity SI environment, SI engineers can experiment with the stack-up, power distribution system (including I/O models), routing, planes, and decoupling capacitors to derive working configurations for implementation.

Constraint-driven design methodology

Allegro Sigrity SI technology works seamlessly with the constraint management system of the Allegro PCB and IC Packaging Design tools. Constraints derived through simulation can be put into an Electrical Constraint Set (EC Set) from within the topology canvas, SigXplorer. These EC Sets can then be applied to other nets in the design through the constraint management system found in Allegro Sigrity SI, Allegro Design Authoring, and Allegro PCB Editor. Designers can use the constraints developed through simulation and exploration, and enable a front- to backend constraint-driven design process.

SI layout checks

Bridging the gap between implementation and analysis, Allegro Sigrity SI provides unique layout checks that utilize fast SI screening algorithms. The trace impedance and coupling checks provide insight into common SI problems without having to run detailed analysis. The trace impedance check can point a designer directly to locations in the layout where the impedance discontinuities are the greatest, such as where a trace has been pushed out over a void area in a power or ground shape on a neighboring layer. If not detected early, such conditions may not be found until final post-route analysis, which could impose a delay on the schedule.

Similarly, the coupling checks point out the largest coupling coefficients on the PCB or IC package design, and allow designers to explore alternative routing schemes to minimize the possibility of a crosstalk error being found during post-route analysis.

While the impedance and coupling checks provide a physical location that should probably be edited, PCB and IC package designers are often faced with the dilemma of bending or breaking design rules in order to get a design completed. To provide an electrical assessment of potentially problematic nets, Allegro Sigrity SI provides SI performance metrics. Without setting up detailed IBIS models, SI performance metric checks can be run on large groups of signals, utilizing time-domain simulation and considering non-ideal power and ground rails. An extensive HTML-based report can be created that will empower the layout designer to assess the physical layout from an electrical standpoint, and address a significant category of SI issues in-design, thus accelerating the design flow.

Benefits

- Pre- and post-route SI analysis integrated with the physical design flow provides optimum methodology
- Rapid evaluation of feasibility, cost, and performance tradeoffs through virtual prototyping environment
- Electrical constraint capture enables constraint-driven physical design methodology
- Scalable crosstalk analysis, from segment-based crosstalk DRCs to detailed time-domain simulation
- Hybrid (2D/3D) and full-wave 3D solvers provide extraction scalability, and enable power-aware SI analysis by extracting a power-distribution system coupled with signals

- Advanced parallel-bus (DDR) and serial-link (SerDes) analysis
- Electrical assessment of IC packages quickly identifies electrical faults and baselines performance metrics
- Includes a SPICE-based simulation engine and embedded integration with hybrid (2D/3D) and full-wave 3D field solvers
- Reads/writes Cadence Allegro PCB (.brd), APD (.mcm) and Digital SiP Layout (.sip) files

Operating System Support

Allegro platform technology:

- Linux
- Windows

Cadence Services and Support

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach more than 70 courses and bring their real-world experience into the classroom
- More than 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- Cadence Online Support gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more

Allegro Sigrity SI Product Summary

Sigrity products	Allegro Sigrity SI Base	Power-Aware SI Option	System Serial Link Option	Package Assessment/ Extraction Option
Broadband SPICE®		•	•	
Transistor to Behavioral Model Conversion		•	•	
CAD Design/Data Translators		•	•	•
PowerDC™				•
PowerSI™		•	•	
PowerSI 3D EM Full-Wave Extraction		•	•	•
SPEED2000™		•		
SystemSI™ - Serial Link Analysis			•	
SystemSI - Parallel Bus Analysis		•		
XtractIM™				•

Note: An option license provides access to one product at a time

Allegro Sigrity SI Feature Summary

Features	Allegro Sigrity SI Base	Power-Aware SI Option	System Serial Link Option	Package Assessment/
IBIS 5.1 support	•	•	•	
Graphical topology editor	•			
Bus-level topology editor		•	•	
Generate estimated crosstalk tables	•			
Detailed HTML simulation reports	•	•	•	•
Differential pair extraction from Allegro Design canvas	•			
Differential pair extraction from Allegro Design Entry HDL	•			
Multi-terminal black boxes in topologies	•	•	•	

Features	Allegro Sigrity SI Base	Power-Aware SI Option	System Serial Link Option	Package Assessment/
Post-layout selection from Allegro PCB Editor	•			
HSPICE interface	•	•	•	
Differential signal constraint capture	•			
Sweep simulations	•	•	•	
Constraint development and capture of topologies	•	•	•	
Constraint-driven floorplanning and placement	•			
Allegro Constraint Manager	•			
Color-coded real-time feedback on violations	•			
Spectre transistor-level model support	•			
Source-synchronous bus analysis		•		
SSN analysis		•		
Batch simulation	•	•	•	
Constraint-driven routing	•			
Allegro route by pick	•			
Thermally-aware static IR drop analysis				•
Time domain simulation of S-parameters	•	•	•	
Coupled via model generator for pre-layout explorations	•	•	•	
High-capacity channel simulation			•	
Optimum pre-emphasis bit configurations (“tap settings”)			•	
BER prediction			•	
Bathtub curves			•	
Channel compliance—statistical analysis			•	
2D (static and full-wave) extraction	•			
Hybrid-solver (2D/3D) extraction		•	•	•
3D full-wave extraction		•	•	•
Signal-quality screening of routed nets	•	•	•	•
Impedance requirements calculator	•			
Frequency domain analysis	•	•	•	•

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