



OrCAD & Allegro V17.4-2019

PCB Design comparison grid

Features	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
• OrCAD CAPTURE SCHEMATIC ENTRY + COMPONENTS DATABASE MANAGEMENT			
Graphical, flat and hierarchical page editor and Picture block hierarchy	•	•	•
OrCAD Capture Market place for Apps, Models, Symbols and more	•	•	•
Net Groups - Complex bus definition	•	•	•
Intelligent PDF creation	•	•	•
AutoWire	•	•	•
44,000 Schematic symbols	•	•	•
Coloured Components / nets	•	•	•
Tcl TK scripting support	•	•	•
Online design rule check including custom DRC capability and Waive DRC	•	•	•
Forward and back-annotation of properties / pin-and-gate swaps	•	•	•
Schematic Part and Library editor	•	•	•
Cross-probing and cross-placing	•	•	•
FPGA design-in / pin import & export	•	•	•
Multiple PCB netlist interfaces	•	•	•
SI Topology creation	•	•	•
Digi-Key (PartLink App) Component Parametric data directly from web	•	•	•
Property editor for pins, components, nets	•	•	•
Constraint Manager (Spacing, Physical, Electrical)	•	•	•

Features	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
Designs Comparison.	•	•	•
Autodesk® Eagle and Altium® import	•	•	•
Export/Import XML	•	•	•
Component Information System	CIS option	CIS option	•
Windows ODBC compatible format	CIS option	CIS option	•
Interface to relational database and management systems	CIS option	CIS option	•
Database query for part selection and parametric properties	CIS option	CIS option	•
Schematic and BOM Variants Manager (Parts not Fitted and more).	CIS option	CIS option	•
CIS Database Management Interface (access control and more)	CIS Option	CIS Option	•
Part search DIGIKEY, FARNELL, FUTURE, MOUSER, ARROW	CIS Option + CIP E options	CIS Option + CIP E options	CIS Option + CIP E option
• PCB EDITOR			
Physical, Spacing, Same net, Netclass and Class to Class rules	•	•	•
Interactive Routing using Working Layer (layer selection popup)	•	•	•
Split View	•	•	•
Multiple placement options, manual, quickplace, auto and room	•	•	•
Placement directly from schematic, individually or window select	•	•	•
Interactive route completion	•	•	•
Component lead editor	•	•	•
Dynamic Shapes (dynamic copper pours) Plow and Heal	•	•	•
Snake Routing for Hex pattern ICs	•	•	•
Scibble Routing	•	•	•
Push, Shove and Hug interactive editing	•	•	•
Embedded net names	•	•	•
Curve Routing	•	•	•
Through Board Transparency (OpenGL)	•	•	•
Multi-line routing (Group Routing)	•	•	•
Fan-out generators	•	•	•
Flip Board	•	•	•
Dynamic pad suppression / Unused Pad removal	•	•	•
Design for Assembly, Fabrication, Test checks	•	•	•

• Function included

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STEP 3D viewer for selected item or complete PCB.	•	•	•
Gerber 274X, 274D artwork Output	•	•	•
Auto Finish (Route Completion Tool)	•	•	•
IPC2581 Import / Export	•	•	•
Mentor ODB++ and universal viewer	•	•	•
DFM Checks including soldermask, solderpaste and more	•	•	•
Route cleanup, optimization (Glossing)	•	•	•
Cross Section Editor	•	•	•
Impedance Calculator	•	•	•
Interactive / Automatic Silkscreen generation	•	•	•
Manual Design For Test (DFT) / Test Prep	•	•	•
Component Height DRC	•	•	•
Associative Dimensioning	•	•	•
Import Files Manager	•	•	•
Import CAD Translators: Mentor® Boardstation, Autodesk® Eagle, Altium®, PADS, PCAD, OrCAD® Layout	•	•	•
MCAD/ECAD Incremental design data exchange (IDX)	•	•	•
Skill Extension Language	•	•	•
Differential Pairs Physical rules and routing	•	•	•
Differential Pair Static Phase Control rules	•	•	•
Differential Pair Dynamic Phase Control rules		•	•
Shape based curve fillet support, tapered traces		•	•
Alignment x and y for components and modules		•	•
Placement replication, template based design reuse		•	•
HighSpeed Analysis Coupling and Impedance		•	•
Constraint Regions, region based rules (Rigid -Flex ; BGA regions)		•	•
Total Etch Length - Max/Min Length		•	•
Interactive Delay Tuning		•	•
Automatic Design For Test (DFT) / Test Prep		•	•
Group route via pattern		•	•
Hug Contour routing		•	•
Via array / Shielding - Shape and Trace based		•	•
Route and Placement Vision		•	•
Net Scheduling, T-Point rules (pin to T-point), T-Point definition		•	•

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Propagation delay rules (Min/Max, Relative) for nets or groups		•	•
Impedance DRC		•	•
Package Pin and Z-axis delay		•	•
Dynamic Heads-up Display for critical rules		•	•
Flex/Rigid design		•	•
Inter Layer check for Flex/Rigid		•	•
Collision detection, place symbols and bending flex in 3D View.		•	•
Backdrilling		•	•
Max Via Count rules			•
Dynamic DFA rules based interactive placement			•
Offset Routing			•
Layer set rules			•
Extended (X)net rules			•
Estimated Crosstalk rules			•
Pin Pair rules			•
Design planning - Create hierarchical Bundles			•
Design planning - Create, Edit Flows			•
Design planning - Assign Flows to Layers			•
Design Planning - Plan Spatial Feasibility analysis & feedback			Design Planning Option
Design Planning - Generate Topological Plan			Design Planning Option
Design Planning - Convert Topological plan to traces (CLINES)			Design Planning Option
Design Planning - Plan Topological with Electrical rules			Design Planning Option
Auto Interactive Delay Tune (AiDT)			PCB High-Speed Option
Electrical Constraint rule set (ECSets) / Topology Apply			PCB High-Speed Option
Electrical rules (Reflection, Timing, Crosstalk)			PCB High-Speed Option
Package Pin Delay (for die-2-die delay) rules			PCB High-Speed Option
Dynamic Differential Pair Phase Control rules			PCB High-Speed Option
Z-Axis delay feedback			PCB High-Speed Option
Extended Net creation			PCB High-Speed Option
Advanced Constraints (formulas, relational)			PCB High-Speed Option
Segment over void detection			PCB High-Speed Option
Spread lines between voids			PCB High-Speed Option
HDI Micro-via (spacing, stacking) rules			Miniaturization Option

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HDI micro-via inset (via-in-pad) rules			Miniaturization Option
HDI micro-via stack editing			Miniaturization Option
Dynamic shape based filleting, line fattening and trace filleting			Miniaturization Option
Single Click multiple micro- via instantiation			Miniaturization Option
Unused micro-via removal			Miniaturization Option
Manufacturing rule support for embedding components			Miniaturization Option
Embedded Packaged Components			Miniaturization Option
Support for Cavities on inner layers			Miniaturization Option
Dual Side Contact Components			Miniaturization Option
Vertically Placed Components			Miniaturization Option
Removal of unassigned indirect attached vias			Miniaturization Option
Concurrent Team Design - Layer by Layer			PCB Team Design Option
Concurrent Team Design - Functional block partitioning			PCB Team Design Option
Concurrent Team Design - Team design dashboard			PCB Team Design Option
Concurrent Team Design - Soft nets			PCB Team Design Option
Concurrent Team Design - Flexible boundaries			PCB Team Design Option
Concurrent Team Design - Constraint Editing per Partition			PCB Team Design Option
Swap pins on a FPGA (based on FPGA rules) in PCB Editor			FPGA System Planner
Reoptimize pins on a FPGA (using FPGA rules)			FPGA System Planner
Parameterized RF etch elements			PCB Analog / RF Option
Asymmetrical Clearances			PCB Analog / RF Option
RF Etch elements editing			PCB Analog / RF Option
Bi-Directional interface with Agilent ADS			PCB Analog / RF Option
ADS schematics Import Agilent into DE-HDL			PCB Analog / RF Option
Layout-driven RF design creation			PCB Analog / RF Option
Flexible Shape Editor			PCB Analog / RF Option
Via Array placement on traces, shapes			PCB Analog / RF Option
• AUTOROUTER			
6 Signal Layers at a time (no board layer limit or pin limit)	•	•	•
Shape-based or Gridded routing	•	•	•
SMD Fanout		•	•
Trace Width by Net and Net Classes		•	•
45-degree / Memory Pattern Routing		•	•

• Function included

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Interactive Routing with Shoving and Plowing		•	•
Interactive Floorplanning		•	•
Online Design Rule Checking		•	•
Flip, Rotate, Align, Push, and Move Components		•	•
Placement Density Analysis		•	•
High-Speed rules based autorouting			•
Min/Max, matched length rules based autorouting			•
Pin-pair rules, Area rules based autorouting			•
Crosstalk controls, parallelism rules based autorouting			•
Differential Pair Autorouting, Automatic net shielding			•
High-speed rules-based autorouting			•
256 signal layer limit			PCB Routing Option
DFM rules-based autorouting			PCB Routing Option
Automatic trace spreading			PCB Routing Option
ATP generation			PCB Routing Option
Layer-specific rules-based autorouting			PCB Routing Option
• SIGNAL INTEGRITY			
Pre- & Post-route signal integrity analysis		•	
Graphical topology definition and exploration		•	
Interactive waveform viewer		•	
Macro modelling support (DML)		•	
IBIS 5,0 support		•	
IBIS ICM model support		•	
Spectre-to-DML		•	
HSPICE-to-IBIS		•	
Lossy transmission lines		•	
Coupled (3 net) simulation		•	
Differential pair exploration and simulation		•	

• Function included

Features	OrCAD PCB Designer Standard	OrCAD PCB Designer Professional	Allegro PCB Designer
• PSpice A/D Basic			
Analysis Types	•	•	
Libraries - Digital Devices	•	•	
Modeling Apps	•	•	
Simulation Capacity	Capacity Limited – 250 nodes	Capacity Limited – 250 nodes	
Libraries – Analog	No advanced analog models supported like BSIM 3.3, 4, Magnetic Cores, IGBT, DMI models, etc	No advanced analog models supported like BSIM 3.3, 4, Magnetic Cores, IGBT, DMI models, etc	
Waveform Analyses	All but Performance Analysis	All but Performance Analysis	

• Function included